ARM

Exam EN0-001

ARM Accredited Engineer

Version: 6.0

[Total Questions: 210]

Question No : 1

A deeply embedded real-time industrial control system is missing some hard real-time interrupt deadlines. Which of the following performance analysis techniques is the most suitable for identifying which routines are causing the problem?

A. Use an ETM instruction trace profiler, which outputs information about the program as it runs
B. Add some serial logging to the software, which outputs information about the program as it runs
C. Add a new interrupt handler, which is triggered off a timer, and dump information about the interrupted process
D. Use a JTAG sample-based profiler, which periodically halts the CPU, and dumps information about the interrupted process

Answer: A

Question No : 2

In a multi-processor system, there are four processors numbered 0, 1, 2 and 3. The state of the processors is as follows:

- CPU 0 and 1 are sleeping in low-power state following a WFI instruction. . CPU 2 is executing program code.
- CPU 3 is sleeping in low-power state following a WFE instruction.

CPU 2 executes a SEV instruction. What is the effect on the system?

A. CPU 0: executing, CPU 1: executing, CPU 2: executing. CPU 3: executing
B. CPU 0: executing, CPU 1: executing. CPU 2: executing. CPU 3: sleeping
C. CPU 0: sleeping, CPU 1: sleeping. CPU 2: executing. CPU 3: executing
D. CPU 0: sleeping, CPU 1: sleeping. CPU 2: sleeping, CPU 3: executing

Answer: C

Question No : 3

Consider the following instruction sequence:

STR r0, [r2] ; instruction A

DSB

ADD r0, r1, r2 ; instruction B

LDR r3, [r4] ; instruction C

SUB r5, r6, #3 ; instruction D

At what point will execution pause until the STR access is complete?

A. After instruction A and before the DSB
B. After the DSB and before instruction B
C. After instruction B and before instruction C
D. After instruction C and before instruction D

Answer: B

Question No : 4

A simple method of measuring the performance of an application is to record the execution time using the clock on the wall or a wristwatch.

When is this method INAPPROPRIATE?

A. When executing the software using a simulation model
B. When the processor is a Cortex-R4
C. When instruction tracing is enabled
D. When the processor is not executing instructions from cache

Answer: A

Question No : 5

When a linker is removing unused sections during a static link (for example, -remove or -gc-sections), it finds the sections to keep by following all relocations starting from:

A. The entry point(s).
B. The function named 'main'.
C. All local functions and variables.

D. The reset vector.

Answer: A

Question No : 6

In which of these cases would code have better performance when compiled for Thumb state than when compiled for ARM state?

A. When the processor has no data cache
B. When the code involves many shifting operations
C. When the code has many conditionally executed instructions
D. When the processor can only fetch instructions 16-bits at a time

Answer: D

Question No : 7

When using a Generic Interrupt Controller (GIC), how does code cause a software-generated interrupt?

A. By executing an SGI instruction
B. By writing to a register in the GIC
C. By writing to the F bit in the CPSR
D. By writing to the I bit in the CPSR

Answer: B

Question No : 8

Processors which implement the ARMv7-A architecture can be configured to allow unaligned memory access. Unaligned accesses have a number of advantages, disadvantages, and limitations.

Which TWO of the following statements are true? (Choose two)

A. Unaligned accesses may take more cycles to execute than aligned accesses

B. Unaligned loads and stores are necessary for accessing fields in packed structures
C. A program compiled using unaligned accesses can be safely executed on all ARMv7-A devices
D. If the relevant control register setting is enabled all loads and stores can function from unaligned addresses
E. Unaligned accesses can only be made to Normal memory

Answer: A,E

Question No : 9

Which of the following instructions can be used to enter a power saving mode?

A. PLD
B. PLI
C. WFE
D. DSB

Answer: C

Question No : 10

According to the AAPCS (with soft floating point linkage), when the caller "func" calls sprintf, where is the value of the parameter "x" placed?

```
#include <stdio.h>

void func(double x, int i , char *buffer)

{

sprintf(buffer, "pass %d: value = %f\n", i, x); }
```

A. Split between register R3 and 4 bytes on the stack
B. Split between registers R3 and R4
C. 8 bytes on the stack
D. VFP Register D0

Answer: C

Question No : 11

When timing a critical function for an algorithm, using platform time functions such as get time of day (), the result is unpredictable; there is significant variance in the measured time between different runs of the benchmark. Which of the following strategies would improve the accuracy of the measurement?

A. Time multiple executions of the algorithm and average the result
B. Break the algorithm into smaller pieces and time them individually
C. Run the code on a software model of the platform and collect the results on that system
D. Add some code with a known overhead to the algorithm to make it run slower, and remove the overhead afterwards

Answer: A

Question No : 12

How many bytes of stack are needed to pass parameters when calling the following function?

int foo(short arg_a, long long arg_b, char arg_c, int arg_d)

A. 0
B. 4
C. 8
D. 15

Answer: C

Question No : 13

Which instruction would be used to return from a Reset exception?

A. MOVS PC, R14
B. MOVSPC, R13

C. Architecturally not defined
D. SUBS PC, R14, #4

Answer: C

Question No : 14

On an ARM processor that does not implement Security Extensions, which one of the following can be the starting address of the exception vector table?

A. 0xFFFFFFFF
B. 0xFFFFFFF0
C. 0xFFFF0000
D. 0x0000FFFF

Answer: C

Question No : 15

In the Generic Interrupt Controller (GIC), when an interrupt is requested, but is not yet being handled, it is in which of the following states?

A. Inactive
B. Active
C. Pending
D. Edge-triggered

Answer: C

Question No : 16

An undefined instruction will cause an Undefined Instruction exception to be taken when:

A. It is fetched.
B. It is decoded.
C. It is executed.
D. It writes back its results.

Answer: C

Question No : 17

The following pseudocode sequence shows a flag being set to indicate that new data is ready to be read by another thread:

data = 123;

ready = true;

Assuming that the reader threads may execute on any other core of a multicore system, which of the following is the most efficient memory barrier to place between the two writes to prevent them being observed in the opposite order?

A. DSBSY
B. DSBST
C. DMBSY
D. DMBST

Answer: D

Question No : 18

Which one of the following statements is TRUE for monitor mode debugging?

A. Monitor mode debug might be suitable for debugging timing critical control software
B. Monitor mode debug only supports hardware breakpoints and watchpoints
C. Monitor mode debug can be used to halt instruction execution on the processor
D. Monitor mode debug is only available for ARM processors with a JTAG debug port

Answer: A

Question No : 19

A Programmer's View CPU model usually provides:

A. Cycle-accurate simulation of the CPU.
B. Instruction-accurate simulation of the CPU.
C. Simulation of user-defined memory-mapped peripherals.
D. Cycle-accurate simulation of the cache and memory system.

Answer: B

Question No : 20

In an ARMv7-A processor that includes the Advanced SIMD extension (NEON), where are the data values operated on by NEON instructions stored?

A. In system memory
B. In registers shared with the VFP register set
C. In registers shared with the integer register set
D. In dedicated registers not shared with other registers

Answer: B

Question No : 21

The following C function is compiled with hard floating point linkage.

float function(int a, float b, int c, float d);

Which register is used to pass argument c?

A. R0
B. R1
C. R2
D. R3

Answer: B

Question No : 22

Which one of the following statements best describes the function of vector catch logic?

A. It traps writes to the memory containing the vector table
B. It provides additional resources for debugging exception handlers
C. It provides configurable exception priorities on an ARM processor
D. It provides an improved mechanism for an application to handle exceptions

Answer: B

Question No : 23

The automatic removal of a cache line from a cache to free the location is known as cache line:

A. Coherency
B. Pre-fetch
C. Eviction
D. Allocation

Answer: C

Question No : 24

In the CPSR, 1=0 and F=1. Which of the following is TRUE in this case?

A. Both IRQs and FIQs are enabled
B. Both IRQs and FIQs are disabled
C. IRQs are disabled and FIQs are enabled
D. IRQs are enabled and FIQs are disabled

Answer: D

Question No : 25

Which of the following statements regarding Strongly-ordered memory is architecturally FALSE?

A. Address locations marked as Strongly-ordered memory are never held in a cache
B. The architecture does not permit speculative data accesses to Strongly-ordered memory